DECLARATION

I, the undersigned, of 10-18, Yokoyama, Shimokaiinji, Nagaokakyo-shi, Kyoto, Japan, hereby certify that I am well acquainted with the English and Japanese languages, that I am an experienced translator for patent matter, and that the attached document is a true English translation of

Japanese Patent Application No. **2003-144480**

that was filed in Japanese.

I declare that all statements made herein of my own knowledge are true, that all statements on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Signature:

Tomoko Yasuda

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Dated: **January 10, 2007**

[Name of the Document] SPECIFICATION

[Title of the Invention] METHOD FOR FABRICATING SEMICONDUCTOR DEVICES

[CLAIMS]

[Claim 1] A method for fabricating semiconductor devices, the method comprising:

the first step of forming a semiconductor layer on a mother substrate;

the second step of forming a metal layer on the semiconductor layer;

the third step of separating the mother substrate from the semiconductor layer;

the fourth step of forming a device isolation region of the semiconductor layer; and

the fifth step of etching the metal layer from the side of the separated mother substrate.

[Claim 2] The method of claim 1, wherein the metal layer is composed of Au, Ag, or Cu.

[Claim 3] The method of claim 1, wherein the metal layer is formed by plating.

[Claim 4] The method of claim 1, wherein the metal layer has a film thickness of 10 μm or more.

[Claim 5] The method of claim 1, wherein the third step is performed by irradiating a side of the semiconductor formed with the mother substrate with a laser.

[Claim 6] The method of claim 1, wherein the third step is performed by polishing.

[Claim 7] The method of claim 1, wherein the fourth step is carried out before the third step.

[Claim 8] The method of claim 1 further comprising the step of bonding a different type of material onto the metal layer before the fifth step.

[Claim 9] The method of claim 8, wherein the different type of material is a polymer material film having an adhesive property.

[Claim 10] The method of claim 9, wherein the polymer material film is composed of a material having a stretching property.

[Claim 11] The method of claim 8, wherein the different type of material is a

semiconductor substrate.

[Claim 12] The method of claim 11, wherein the semiconductor substrate has a cleaving property.

[Claim 13] The method of claim 11 or 12, wherein the semiconductor substrate is used as a heat sink.

[Claim 14] The method of claim 13, wherein the semiconductor substrate is composed of Si or SiC.

[Claim 15] The method of claim 11, wherein after the fifth step, a device isolation region of the semiconductor substrate is etched to have a trench.

[Claim 16] The method of any one of Claims 1 through 15, wherein the semiconductor layer contains Ga and N.

[Detailed Description of the Invention]

[Technical Field to which the Invention Belongs]

The present invention relates to a method for fabricating nitride semiconductor light-emitting devices which emit light in blue-to-ultraviolet regions.

[Prior Art]

Currently, light-emitting diodes each using a group III nitride have been widely commercialized for various types of displays, large-scale displays, signal lights, or the like. In addition, white LEDs each composed of a combination of a GaN LED and a fluorescent material have also been commercialized and expected to replace lighting devices used at present provided that the light emission efficiencies thereof will be improved in future.

In general, a group III nitride semiconductor has been formed on a sapphire substrate as mainstream practice. However, since the sapphire substrate has no conductivity, it is necessary to form a p-type electrode and an n-type electrode on the same plane in a GaN growth layer. This causes the problem of increased series resistance and the problem of increased device size. To solve the foregoing problems, a laser lift-off (hereinafter referred to as LLO) technology has been developed.

The LLO technology is a method which grows a GaN layer on a sapphire substrate and irradiates the side of the GaN layer formed with the sapphire substrate with a laser to thermally decompose the portion of the GaN layer located in proximity to the interface between the GaN layer and the sapphire substrate and thereby separate the sapphire substrate from the GaN layer.

A description will be given herein below to a known method for fabricating semiconductor devices using the LLO technology with reference to FIGS. **7**. This known method is disclosed in Patent Document 1. A GaN layer **102** is deposited on a sapphire substrate **101** (see FIG. **7(a)**). Next, an electrode layer **103** is formed on the GaN layer **102** and then insulating films **104** are formed on specified regions of the electrode layer **103** (see FIG. **7(b)**). Next, a Cu plate **105** with a thickness of about 50 μm is formed on the electrode layer **103**. In this case, Cu is not plated on the insulating films **104**, while the Cu plate **105** having a configuration as shown in FIG. **7(c)** is formed on the electrode layer **103**. Next, a holding metal **106** is formed over the Cu plate **105** (see FIG. **7(d)**). Next, the sapphire substrate **101** is separated from the GaN layer **102** by using the LLO technology. Then, electrode layers **107** are formed on specified regions of the GaN layer **102**. Subsequently, the holding metal **106** is separated from the Cu plate **105** (see FIG. **7(e)**). In FIG. **7(e)** and also in FIG. **7(f)**, the orientation of the drawing has been vertically inverted from that of the drawing in each of the other drawings. Next, the GaN layer **102** is scribed to be cleaved such that individual chips are separated from each other. In this case, since the bonded portion **106** of the Cu plate **105** is relatively low in bonding strength, the Cu plate **105** is also easily separated by cleaving the GaN layer **102** (see FIG. **7(f)**).

A description will be given to another known method for fabricating semiconductor devices using the LLO technology with reference to FIGS. **8**. This known method is disclosed in Patent Document 2. A GaN layer **102** is deposited on a sapphire substrate **101** (see FIG. **8(a)**). Next, an electrode layer **104** is formed on the GaN layer **102** and then an Au plate **105** with a thickness of 10 μm or more is formed thereon (see FIG.

8(b)). Next, the sapphire substrate **101** is separated from the GaN layer **102** by using the LLO technology (see FIG. **8(c)**). Next, electrode layers **107** are formed on the exposed surface of the GaN layer **102** (see FIG. **8(d)**). Next, a resist mask **108** is formed on the Au plate **105** and then the Au plate **105** is patterned such that the portion of the Au plate **105** serving as a chip isolation region is removed (see FIG. **8(e)**). In this case, the portion of the Au plate **105** is removed by performing wet etching with respect to the surface of the Au plate **105** opposite to the surface thereof in contact with the GaN layer **102**. Next, the resist mask **108** is removed by organic cleaning. Then, the GaN layer **102** is cleaved or cut by using a dicing blade such that the individual chips are separated from each other (see FIG. **8(f)**).

Thus, the nitride semiconductor devices have been fabricated by using the LLO technology as shown in the foregoing methods.

[Patent Document 1]

Japanese Laid-Open Patent Publication No. 2001-274507

[Patent Document 2]

Japanese Patent Application No. 2002-183919

[Problems that the Invention is to solve]

However, the known methods for fabricating semiconductor devices encounter the following problems. First, in the method illustrated in FIGS. **7**, the function of the thin-film GaN layer **102** as a holding member is degraded if the bonding strength of the Cu plate is extremely low. Consequently, there are cases where the GaN layer **102** is naturally split in the first and second cleavage steps. Since such naturally split chips mostly have rough and uneven surfaces, they cannot be used as devices, which causes a reduction in yield. Conversely, if the bonding strength of the Cu plate is high, there are cases where the Cu plate is not separated even when the GaN layer **102** is separated by cleavage, which also causes a reduction in yield. Thus, the method illustrated in FIGS. **7** requires strict control of the bonding strength of the Cu plate.

In the method illustrated in FIGS. **8**, the resist mask is formed on the thick-film Au plate in the step illustrated in FIG. **8(d)**. If the film thickness of the Au plate is large, however, it is difficult to recognize a pattern of an underlie for the Au plate so that mask alignment becomes difficult, which causes a reduction in yield. There are also cases where the thin-film GaN layer **102** is naturally separated at the stage at which the portion of the Au plate has been removed, which also causes a reduction in yield in the same manner as described above. Thus, it is also difficult to achieve a high yield even in accordance with the method illustrated in FIGS. **8**.

[Means of Solving the Problems]

In order to solve the above problems, a method for fabricating semiconductor devices of the present invention includes: the first step of forming a semiconductor layer on a mother substrate; the second step of forming a metal layer on the semiconductor layer; the third step of separating the mother substrate from the semiconductor layer; the fourth step of forming a device isolation region of the semiconductor layer; and the fifth step of etching the metal layer from the side of the separated mother substrate.

With this structure, devices are separated by etching the metal layer. This can prevent a yield from being reduced due to the causes described in [Problems that the Invention is to solve]. A resist pattern is formed not on the metal layer but on the semiconductor layer, and then etching is performed with respect to the metal layer from the side of the semiconductor layer in contact with the mother substrate. This makes it very easy to perform mask alignment, leading to the improved yield.

In the method of the present invention, the metal layer is preferably composed of Au, Ag, or Cu.

In the method of the present invention, the metal layer is preferably formed by plating.

In the method of the present invention, the metal layer preferably has a film thickness of 10 μm or more.

In the method of the present invention, the third step is preferably performed by irradiating a side of the semiconductor formed with the mother substrate with a laser.

In the method of the present invention, the third step is preferably performed by polishing.

In the method of the present invention, the fourth step is preferably carried out before the third step. This preferable structure can prevent the splitting of a wafer during the LLO process and improve the yield.

It is preferable that the method of the present invention further includes the step of bonding a different type of material onto the metal layer before the fifth step.

In the method of the present invention, the different type of material is preferably a polymer material film having an adhesive property.

In the method of the present invention, the polymer material film is preferably composed of a material having a stretching property. With this preferable structure, the different type of material can also be used as an expand sheet so that the number of fabrication process steps can be reduced.

In the method of the present invention, the different type of material is preferably a semiconductor substrate. This preferable structure enhances the ability to hold the thin-film GaN layer after the LLO process and allows chips to be separated from each other with an excellent yield.

In the method of the present invention, the semiconductor substrate preferably has a cleaving property. This preferable structure can facilitate isolating devices from each other and improve the yield.

In the method of the present invention, the semiconductor substrate is preferably used as a heat sink when semiconductor devices are mounted on the semiconductor substrate. This preferable structure can simplify the mounting step.

In the method of the present invention, the semiconductor substrate is preferably composed of Si or SiC.

In the method of the present invention, after the fifth step, a device isolation region of the semiconductor substrate is preferably etched to have a trench. This preferable structure can facilitate the cleavage of the semiconductor substrate and improve the yield.

In the method of the present invention, the semiconductor layer preferably contains Ga and N.

[Embodiments of the Invention]

Referring to the drawings, the individual embodiments of the present invention will be described herein below.

(EMBODIMENT 1)

Referring to FIGS. **1**, a method for fabricating blue surface emitting devices each composed of a nitride semiconductor according to a first embodiment of the present invention will be described.

As a system for growing a GaN layer, a MOVPE (metal organic vapor phase epitaxy) system is used. As a Ga raw material, trimethylgallium is used, while NH_3 is used as an N raw material. As an Si raw material serving as a donor impurity, SiH_4 is used, while H_2 is used as a carrier gas.

First, a low-temperature buffer layer is formed on a 2-inch (0001) sapphire substrate **1**. Then, an n-type GaN layer **2** is grown on the low-temperature buffer layer to have a film thickness of 4 μm. In this case, a growth temperature for the GaN layer **2** is 1030 °C. Subsequently, the carrier gas is switched to N_2 and the growth temperature is reduced to 800 °C so that an active layer **3** made of InGaN is grown on the GaN layer **2** to have a film thickness of 20 nm. In the present embodiment, blue light at a wavelength of 470 nm is emitted from the active layer **3** made of InGaN. As an In raw material, trimethylindium is used. Although the present embodiment has assumed the case where the active layer **3** has an SQW structure, the active layer **3** may also have an MQW structure instead. Then, the growth temperature is increased again to 1020 °C such that a p-type GaN layer **4** is grown on the active layer **3** to have a film thickness of 0.8 μm. As an Mg raw

material which is an acceptor impurity, cyclopentadienylmagnesium is used (see FIG. **1(a)**).

Next, a p-type GaN layer **4** is grown as the uppermost layer and then annealing is performed in a nitrogen atmosphere at 750 °C for 20 minutes by using an annealing system such that the resistance is further lowered.

After annealing, Ni/Au multilayer films are formed as p-type contact electrodes **5** by EB vapor deposition on the p-type GaN layer **4** (see FIG. **1(b)**). Thereafter, sintering is performed in an oxygen atmosphere at 500 °C.

Next, after the formation of the p-type contact electrodes **5**, a Ti/Au multilayer film is formed as an underlying film **6** for Au plate by EB vapor deposition over the entire surface of the sample. Thereafter, an Au plate **7** is formed on the underlying film **6** to have a film thickness of 30 μm (see FIG. **1(c)**). The Au plate **7** operates as a member for holding the n-type GaN layer **2** when the sapphire substrate **1** is removed from the n-type GaN layer **2** having a film thickness of about 5 μm in a subsequent step. The holding ability of the Au plate **7** increases as the film thickness thereof becomes larger but an excessively large film thickness degrades the heat releasing property of each of the devices. Accordingly, the film thickness of the Au plate **7** is preferably in the range of about 10 to 150 μm. As stated previously, the present embodiment has adjusted the film thickness of the Au plate **7** to 30 μm. As the material of a metal layer having a large film thickness, a material having a high heat conductivity is preferred. Besides Au, Ag or Cu can be listed as a candidate for the material. Although in the present embodiment the metal layer has been formed by plating, it may also be formed by a method other than plating.

After the formation of the Au plate **7**, the sapphire substrate **1** is removed from the n-type GaN layer **2** (see FIG. **1(d)**). As a method for removing the sapphire substrate **1**, a polishing process, a laser lift-off (LLO) process, or the like may be used. Since the sapphire substrate **1** is extremely firm and solid, the removal of the sapphire substrate **1** using a polishing process has the problem that it requires a long time and it is difficult to

control. In view of the problem, the present embodiment has removed the sapphire substrate **1** by using the laser lift-off process. Specifically, the portion of the n-type GaN layer **2** located in proximity to the interface between the n-type GaN layer **2** and the sapphire substrate **1** is thermally decomposed by irradiating the back surface of the sapphire substrate **1** with a YAG laser so that the sapphire substrate **1** is separated from the n-type GaN layer **2**. After the laser lift-off process, a Ga metal resulting from the decomposition is adhered to the portion of the n-type GaN layer **2** located in proximity to the interface so that it is removed by using a hydrochloric acid.

Next, a mask is formed on the exposed surface of the n-type GaN layer **2** from which the sapphire substrate **1** has been removed and then the portions of the nitride semiconductor layers which are present in the chip isolation region of each of the n-type GaN layer **2**, the active layer **3**, and the p-type GaN layer **4** are removed completely by dry etching. Thereafter, the used mask is removed (see FIG. **1(e)**). The orientation of the drawing in FIG. **1(d)** has been vertically inverted from that of the drawing in FIG. **1(e)**. As an etching gas for dry etching, a Cl-based gas, e.g., is used. The mask is preferably composed of a material resistant to dry etching, such as a dielectric film made of SiO_2 or the like or a metal film made of Ni or the like. In the case of using a resist, the resist preferably has a large film thickness. In this embodiment, the width of the chip isolation region is 15 μm.

After dry etching, an SiO_2 film **8** is formed, as a passivation film, over the entire surface of the sample. CVD or sputtering is used as a method for forming an SiO_2 film **8**.

After the formation of the SiO_2 film **8**, the portions of the passivation film **8** corresponding to the light extraction portions of the devices are removed. Thereafter, Ti/Au multilayer films are formed as n-type electrodes **9** on the exposed portions of the n-type GaN layer **2** from which the passivation film **8** has been removed (see FIG. **1(f)**). Sintering is performed in a nitrogen atmosphere at 500 °C. As the n-type electrodes **9**, transparent electrodes made of ITO, β-Ga_2O_3, or the like may also be used.

After sintering of the n-type electrodes **9**, a resist mask **10** is formed entirely over the passivation film **8**, the n-type GaN layer **2**, and the n-type electrodes **9** and then opened in a part of the chip isolation region of the resist mask **10**. In the present embodiment, only the center portion of the chip isolation region which corresponds to 5 μm is opened, while the chip isolation region has a width of 15 μm. Then, a sheet **11** is adhered onto a surface of the Au plate **7** (see FIG. **1(g)**). The sheet **11** prevents the individual chips, which are to be separated in a subsequent step, from falling apart. The sheet **11** is composed of a polymer material film and has an adhesive property. By using a polymer film having a stretching property as the sheet **11**, the sheet **11** can also be used as an expand sheet after the completion of the devices so that the number of fabrication process steps is reduced. The sheet **11** may also be attached immediately before or after the LLO process. The arrangement enhances the ability to hold the GaN growth layer during the LLO process or in the process of forming the n-type electrodes **9**.

After the formation of the resist mask **10**, the portion of the SiO_2 film **8** and the portion of the Ti film forming the underlying film **6** for the Au plate are removed. Then, etching is performed with respect to the Au plate **7** by using iodine to provide mutually separated chips. Thereafter, the resist mask **10** is removed, whereby the blue LEDs are fabricated (see FIG. **1(h)**).

Thus, in the present embodiment, the indiscrete Au plate is used as a holding member, and device separation is performed not by cleavage but by removing the Au plate by wet etching. Cleavage for device separation has encountered the problem that the nitride semiconductor layers each having a small film thickness are naturally split or the plate layer remains in an indiscrete state and, as a result, device separation cannot be accomplished. However, the present embodiment can solve the problem and improve the yield. When the Au plate is etched, a resist pattern is formed on the nitride semiconductor layers, the nitride semiconductor layers are patterned, and then etching is performed with respect to the Au plate from the side of the nitride semiconductor layers in contact with the

sapphire substrate. This makes it easier to perform mask alignment than in the known art in which the resist pattern is formed on the Au plate, leading to the improved yield.

This allows the fabrication of blue LEDs with an excellently high yield. Each of the fabricated devices has an extremely excellent heat releasing property since heat is released through the thin-film Au plate with a thickness of 30 μm.

Although the present embodiment has described the case where GaN is grown on sapphire, the present invention is also applicable to each of a substrate and a growth layer composed of other semiconductor materials.

(EMBODIMENT 2)

Referring to FIGS. **2**, a method for fabricating blue surface emitting devices each composed of a nitride semiconductor according to a second embodiment of the present invention will be described.

First, the steps of successively depositing the n-type GaN layer **2**, the active layer **3**, and the p-type GaN layer **4** on the sapphire substrate **1** and performing annealing are performed in the same manner as in the first embodiment (see FIG. **2(a)**).

Next, after annealing, the portions of the nitride semiconductor layers which are present in the chip isolation region of each of the n-type GaN layer **2**, the active layer **3**, and the p-type GaN layer **4** are etched away (see FIG. **2(b)**). In this case, dry etching such as RIE or ECR is performed preferably as an etching process. As an etching gas, a chlorine-based gas is used preferably.

After dry etching, an SiO_2 film **8** is formed, as a passivation film, over the entire surface of the sample. CVD or sputtering is used as a method for forming an SiO_2 film **8**.

After the formation of the SiO_2 film **8**, the SiO_2 film **8** is partially removed. Subsequently, Ni/Au multilayer films are formed as the p-type electrodes **5** by EB vapor deposition on the exposed portions of the p-type GaN layer **4** from which the SiO_2 film **8** has been removed (see FIG. **2(c)**). Thereafter, sintering is performed in an oxygen atmosphere at 500 °C.

After the sintering of the p-type electrode **5**, a Ti/Au multilayer film is formed as the underlying film **6** for Au plate by EB vapor deposition over the entire surface of the sample and then the Au plate **7** is formed on the underlying film **6** to have a film thickness of 30 μm (see FIG. **2(d)**). The Au plate **7** operates as a member for holding a thin-film nitride semiconductor layer when the sapphire substrate is removed from the thin-film nitride semiconductor layer in a subsequent step.

Next, after the formation of the Au plate **7**, the sapphire substrate **1** is removed from the n-type GaN layer **2** (see FIG. **2(e)**). As a method for removing the sapphire substrate **1**, a laser lift-off (LLO) process is used. After the LLO process, a Ga metal resulting from the decomposition is adhered to the portion of the n-type GaN layer **2** located in proximity to the interface so that it is removed by using a hydrochloric acid. Thus, the present embodiment has performed dry etching prior to the LLO process so that the n-type GaN layer **2** has been divided into parts each of a size corresponding to one device when the LLO process is performed. When the sapphire substrate **1** is separated from the n-type GaN layer **2** having a large area of 2 inches as in the first embodiment, the n-type GaN layer **2** is prone to splitting during the LLO process so that a margin for laser irradiation conditions is extremely reduced. By contrast, the present embodiment separates the sapphire substrate **1** from each of the parts of the n-type GaN layer **2** corresponding to one device by the laser lift-off process. This allows the provision of a large margin for laser irradiation conditions and improves the yield.

After the separation of the sapphire substrate **1**, Ti/Au multilayer films are formed as the n-type electrodes **9** by EB vapor deposition on the exposed surface of the n-type GaN layer **2** (see FIG. **2(f)**). The orientation of the drawing in each of FIGS. **2(e)** has been vertically inverted from that of the drawing in FIG. **2(f)**. After the formation of the n-type electrodes **9**, sintering is performed in an N_2 atmosphere at 600 °C.

After sintering, the resist mask **10** is formed to cover the n-type electrodes **9** (see FIG. **2(g)**). Subsequently, the sheet **11** having an adhesive property is adhered onto a

surface of the Au plate **7**. The respective device isolation regions of the passivation film **8** and the Ti film forming the underlying film **6** are removed by using BHF and then etching is performed with respect to the Au plate **7** by using iodine, thereby providing two mutually separated chips. Thereafter, the resist mask **10** is removed by, e.g., organic cleaning, whereby the blue LEDs are fabricated.

Thus, in the present embodiment, like the first embodiment, the indiscrete Au plate is used as a holding member, and device separation is performed not by cleavage but by removing the Au plate by wet etching. Cleavage for device separation has encountered the problem that the nitride semiconductor layers each having a small film thickness are naturally split or the plate layer remains in an indiscrete state and, as a result, device separation cannot be accomplished. However, the present embodiment can solve the problem and improve the yield. When the Au plate is etched, a resist pattern is formed on the nitride semiconductor layers, the nitride semiconductor layers are patterned, and then etching is performed with respect to the Au plate from the side of the nitride semiconductor layers in contact with the sapphire substrate. This makes it easy to perform mask alignment, leading to the improved yield. In addition, the nitride semiconductor layers have been divided by dry etching into parts each of a size corresponding to one device when the LLO process is performed. This prevents the splitting of a wafer during the LLO process and improves the yield.

The following process steps are sequentially carried out: the step of removing an device isolation region of the nitride semiconductor layer by dry etching; the step of removing the sapphire substrate by the LLO process; and the step of etching away a portion of the Au plate from the side of the nitride semiconductor layers in contact with the sapphire substrate. This allows the fabrication of blue LEDs with an excellently high yield. Each of the fabricated devices as in the first embodiment has an extremely excellent heat releasing property since heat is released through the thin-film Au plate with a thickness of 30 μm.

(EMBODIMENT 3)

Referring to FIGS. **3**, a method for fabricating blue surface emitting devices each composed of a nitride semiconductor according to a third embodiment of the present invention will be described.

A method for fabricating blue surface emitting devices according to this embodiment is illustrated in FIGS. **3**. As a system for growing a GaN layer, a MOVPE (metal organic vapor phase epitaxy) system is used. As a Ga raw material, trimethylgallium is used. As an Al raw material, trimethylaluminum is used, while NH_3 is used as an N raw material. As an Si raw material serving as a donor impurity, SiH_4 is used, while H_2 is used as a carrier gas. As an Mg raw material serving as an acceptor impurity, cyclopentadienylmagnesium is used.

First, the low-temperature buffer layer is formed on the 2-inch (0001) sapphire substrate **1**. Then, an n-GaN layer, an n-$Al_{0.15}Ga_{0.85}N$ clad layer, an n-$Al_{0.07}Ga_{0.93}N$ guide layer, an MQW active layer **3** made of InGaN, a p-$Al_{0.07}Ga_{0.93}N$ guide layer, a p-$Al_{0.15}Ga_{0.85}N$ clad layer, and a p-GaN contact layer are sequentially stacked. In FIG. 3(a), the low-temperature buffer layer is not shown, an n-type layer **2a** is composed of the n-GaN layer, the n-$Al_{0.15}Ga_{0.85}N$ clad layer, and the n-$Al_{0.07}Ga_{0.93}N$ guide layer, and a p-type layer **4a** is composed of the p-$Al_{0.07}Ga_{0.93}N$ guide layer, the p-$Al_{0.15}Ga_{0.85}N$ clad layer, and the p-GaN contact layer. In the present embodiment, blue light at a wavelength of 405 nm is emitted from the active layer **3** made of InGaN (see FIG. **3(a)**).

After the above layers are formed, the portions of the nitride semiconductor layers which are present in the chip isolation region of each of the n-type layer **2a**, the active layer **3**, and the p-type layer **4a** are completely etched away (see FIG. **3(b)**). In this case, dry etching such as RIE or ECR is performed preferably as an etching process. As an etching gas, a chlorine-based gas is used preferably.

Next, an SiO_2 film **8** is formed over the entire surface of the sample and then the SiO_2 film **8** is partially removed by BHF (see FIG. **3(c)**). Subsequently, Ni/Au electrodes

are formed as the p-type electrodes **5** on the portions of the p-type layer **4a** other than the optical waveguides and exposed as a result of the removal of the SiO_2 film **8**. Thereafter, sintering is performed in an oxygen atmosphere at 500 °C.

After the sintering, dielectric DBR mirrors **12** are formed on the portions of the p-type layer **4a** which are exposed and will serve as the optical waveguides. The dielectric DBR mirrors **12** are constructed to have a reflectivity of 99.5% or more with respect to light at a wavelength of 405 nm (see FIG. **3(d)**).

After the formation of the dielectric DBR mirrors **12**, a Ti/Au film is formed as the underlying film **6** for Au plate by using an EB vapor deposition apparatus and then the Au plate **7** is formed on the underlying film **6**. The Au plate is set to have a film thickness of 30 μm as in the first and second embodiments (see FIG. **3(e)**).

After the formation of the Au plate **7**, the sapphire substrate **1** at the back surface of the sample is removed (see FIG. **3(f)**). As a method for removing the sapphire substrate **1**, a laser lift-off (LLO) process is used. After the laser lift-off process, a Ga metal resulting from the decomposition is adhered to the portion of the n-type layer **2a** located in proximity to the interface so that it is removed by using a hydrochloric acid.

After the removal of the sapphire substrate **1**, Ti/Au films are formed as the n-type electrodes **9** by EB vapor deposition on the surface portions of the n-type layer **2a** other than the optical waveguides. Thereafter, sintering is performed in a nitrogen atmosphere at 500 °C.

After the sintering, dielectric DBR mirrors **13** are formed on the surface portions of the n-type layer **2a** corresponding to the optical waveguides (see FIG. **3(g)**). The orientation of the drawing in FIG. **3(f)** has been vertically inverted from that of the drawing in FIG. **3(g)**. The dielectric DBR mirrors **13** are constructed to have a reflectivity of 99% or more with respect to a wavelength of 405 nm. Although in the present embodiment the DBR mirrors are formed on the n-type layer by using a dielectric material, the DBR mirrors may also be formed by using growth layers and the difference between the

respective refractive indices of AlGaN materials having different compositions.

After the formation of the dielectric DBR mirrors **13**, a resist mask **10** is formed to cover the n-type electrodes **9** and the dielectric DBR mirrors **13** and expose only part of the chip isolation region. Subsequently, the sheet **11** having an adhesive property is adhered onto the surface of the Au plate **7** (see FIG. **3(h)**).

Thereafter, the respective portions of the SiO_2 film **8** and the Ti film forming the underlying film **6** which correspond to the device isolation region are removed by using BHF and then etching is performed with respect to the Au plate **7** by using iodine, thereby providing two mutually separated chips. Thereafter, the resist mask **10** is removed by, e.g., organic cleaning, whereby the blue LEDs are fabricated (see FIG. **3(i)**).

Thus, in accordance with the method for fabricating semiconductor devices according to the third embodiment, blue LEDs can be fabricated with high yield as in the first and second embodiments.

(EMBODIMENT 4)

A method for fabricating field effect transistors each composed of a nitride semiconductor according to a fourth embodiment of the present invention will be described with reference to FIGS. **4**.

First, an n-type GaN layer **14** and an undoped GaN layer **15** are formed successively on the sapphire substrate **1** by MOCVD (see FIG. **4(a)**). Each of these growth layers has a typical film thickness of about 2 to 3 μm.

Next, the regions of the GaN layers **14** and **15** each of which serves as a device isolation region are completely removed by dry etching (see FIG. **4(b)**). As an etching gas for dry etching, a chlorine-based gas, e.g., is used.

After dry etching, an underlying film **6** for Au plate and an Au plate **7** are formed (see FIG. **4(c)**). The Au plate **7** is set to have a film thickness of 30 μm.

Next, the sapphire substrate **1** is removed by a laser lift-off (LLO) process. After the laser lift-off process, a Ga metal resulting from the decomposition is adhered to the

n-type GaN layer **14** so that it is removed by using a hydrochloric acid (see FIG. **4(d)**).

After the removal of the sapphire substrate **1**, source electrodes **16** and drain electrodes **17** each composed of, e.g., a Ti/Al film and gate electrodes **18** each composed of, e.g., a Pt/Au film are formed on the exposed surface of the n-type GaN layer **14** by the lift-off process (see FIG. **4(e)**). To improve the high-frequency characteristics, a gate length should be shortened to a value of 0.5 μm or less.

Next, the resist mask **10** is formed to cover the source electrodes **16**, the drain electrodes **17**, and the gate electrodes **18**. Subsequently, the sheet **11** having an adhesive property is adhered onto the Au plate **7** (see FIG. **4(f)**).

Next, the portion of the Ti film forming the underlying film **6** which corresponds to the device isolation region is subjected to wet etching by using HF, thereby providing two mutually separated chips. Thereafter, the resist mask **10** is removed by, e.g., organic cleaning, whereby the field effect transistors are fabricated (see FIG. **4(g)**). Each of the fabricated devices has an extremely excellent heat releasing property since heat is released through the thin-film Au plate.

Thus, the method for fabricating semiconductor devices according to the fourth embodiment includes the steps of removing a portion of the nitride semiconductor layer corresponding to the device isolation region by dry etching, forming an Au plate, removing the sapphire substrate by the LLO process, and removing the Au plate from the side of the nitride semiconductor layers in contact with the sapphire substrate. This allows fabrication of transistors with a high yield and excellent heat releasing property.

(EMBODIMENT 5)

A method for fabricating blue surface emitting devices each composed of a nitride semiconductor according to a fifth embodiment of the present invention will be described with reference to FIGS. **5**.

The steps inclusive of and precedent to the step of forming a p-type contact electrode **5** and sintering the same are the same as described above in the second

embodiment (see FIG. **5(a)**).

Next, a Ti/Au film is formed as the underlying film **6** for Au plate and then the Au plate **7** is formed on the underlying film **6** (see FIG. **5(b)**). Then, an Si substrate **19** is bonded onto the Au plate **7** for the purpose of enhancing the ability to hold the thin-film nitride semiconductor layer after a laser lift-off process. Although a method in which the Si substrate **19** is bonded directly to the nitride semiconductor layer without intervention of the Au plate **7** may also be considered, it involves the risk that strain present in the Si substrate **19** is applied to the nitride semiconductor layer to degrade the characteristics of the devices. In view of the risk, the Au plate is formed on the nitride semiconductor layers, and the Si substrate is bonded onto the Au plate. In this case, it is sufficient for the Au plate to function as a buffer material in bonding the Si substrate **19** and therefore have a small film thickness. In the present embodiment, the thickness of the Au plate **7** has been adjusted to 10 μm. The substrate to be bonded preferably has a cleaving property and an excellent heat releasing property. Besides the Si substrate, a SiC substrate or the like is used preferably.

After bonding of the Si substrate **19**, the sapphire substrate **1** is removed by the LLO process (see FIG. **5(c)**).

After the removal of the sapphire substrate **1**, Ti/Au films are formed as the n-type electrodes **9** by EB vapor deposition on the exposed surface of the n-type GaN layer **2** (see FIG. **5(d)**). The orientation of the drawing in FIG. **5(c)** has been vertically inverted from that of the drawing in FIG. **5(d)**. After the formation of the n-type electrodes **9**, sintering is performed in a nitrogen atmosphere at 500 °C.

After the sintering, the resist mask **10** is formed to expose a portion of the n-type electrodes **9** corresponding to only part of the chip isolation region (see FIG. **5(e)**). The respective portions of the SiO_2 film **8** and the Ti film forming the underlying film **6** which correspond to the device isolation region are removed by using BHF. After the removal of the Ti film, the Au plate **7** is removed by etching using iodine. The reason for removing the

Au plate **7** is that the Au plate **7** is in an indiscrete state without being separated when cleavage is performed in a subsequent step. Thereafter, the resist mask **10** is removed by, e.g., organic cleaning (see FIG. **5(f)**). Finally, the Si substrate **19** is polished till the film thickness thereof reaches 120 μm. Then, the Si substrate **19** is cleaved, whereby blue LEDs are fabricated (see FIG. **5(g)**).

Methods for further improving the yield include the following method. After the removal of the Au plate 7 (see FIG. **6(a)**), a trench **20** is formed in the Si substrate **19** by performing wet etching with respect to the exposed part of Si substrate **19** corresponding to the device isolation region (see FIG. **6(b)**). By thus forming the trench **20**, the cleavage of the Si substrate **19** occurs along the trench **20** so that a shift in cleavage position prevents a reduction in yield. Thereafter, the resist mask **10** is removed by, e.g., organic cleaning in the same manner as in the step described above.

Since in the present embodiment the Si substrate is bonded onto the Au plate, the ability to hold the thin-film nitride semiconductor layers after the laser lift-off process is enhanced so that the yield is improved. In addition, the fabricated devices are formed on the Si substrate so that it is no more necessary to attach a heat sink in a mounting step and the mounting step is thereby simplified.

In accordance with the above-mentioned method, blue LEDs can be fabricated with an excellent yield, and the mounting step is simplified.

[Effects of the Invention]

A method for fabricating semiconductor devices of the present invention includes the steps of etching away a portion of a semiconductor layer corresponding to a device isolation region of a substrate, forming an Au plate as a holding member, removing the substrate, and forming a pattern on the semiconductor layer and etching the Au plate from the side thereof in contact with the semiconductor. This allows the fabrication of semiconductor devices with an excellent yield.

[Brief Description of the Drawings]

[FIG. 1] FIGS. **1** are cross-sectional views illustrating a method for fabricating compound semiconductor devices according to a first embodiment of the present invention.

[FIG. 2] FIGS. **2** are cross-sectional views illustrating a method for fabricating compound semiconductor devices according to a second embodiment of the present invention.

[FIG. 3] FIGS. **3** are cross-sectional views illustrating a method for fabricating compound semiconductor devices according to a third embodiment of the present invention.

[FIG. 4] FIGS. **4** are cross-sectional views illustrating a method for fabricating compound semiconductor devices according to a fourth embodiment of the present invention.

[FIG. 5] FIGS. **5** are cross-sectional views illustrating a method for fabricating compound semiconductor devices according to a fifth embodiment of the present invention.

[FIG. 6] FIGS. **6** are cross-sectional views illustrating the method for fabricating compound semiconductor devices according to the fifth embodiment.

[FIG. 7] FIGS. **7** are cross-sectional views illustrating a known method for fabricating semiconductor devices.

[FIG. 8] FIGS. **8** are cross-sectional views illustrating another known method for fabricating semiconductor devices.

[Name of the Document] ABSTRACT

[Summary]

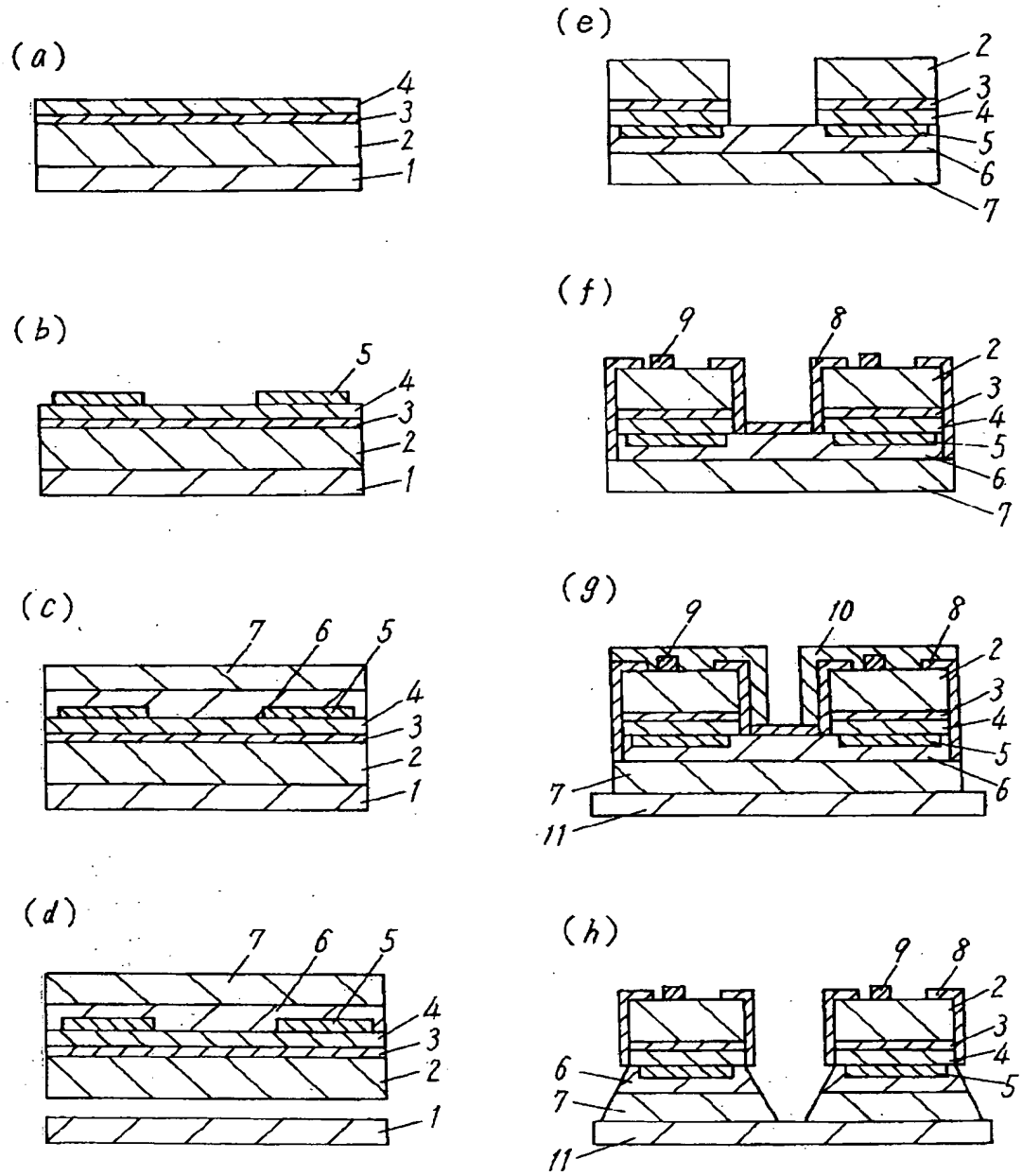
[Purpose] To improve the yield in a semiconductor device process using a known laser lift-off process.

[Solution] A low-temperature buffer layer, an n-type GaN layer **2**, an InGaN active layer **3**, and a p-type GaN layer **4** are grown on a sapphire substrate **1**. Thereafter, the substrate **1** is annealed, thereby lowering the resistance of the p-type GaN layer **4** serving as the uppermost layer. Subsequently, p-type contact electrodes **5** are formed on the p-type GaN layer **4**, and then an underlying film **6** for Au plate and an Au plate **7** with a thickness of 10 through 150 μm are formed. Thereafter, the sapphire substrate **1** at the back surface of a sample is removed, and then the portions of the nitride semiconductor layers which are present in the chip isolation region of each of the n-type GaN layer **2**, the active layer **3**, and the p-type GaN layer **4** are removed. Thereafter, the sample having a part of the chip isolation region exposed is bonded to a sheet **11**, thereby providing mutually separated chips.

[Selected Figure] FIG. **1**

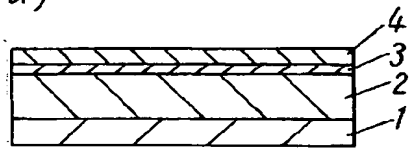
【書類名】 図面 [Name of the Document] DRAWINGS

【図1】 [FIG. 1]



[図2] [FIG. 2]

(a)



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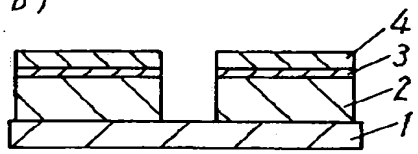

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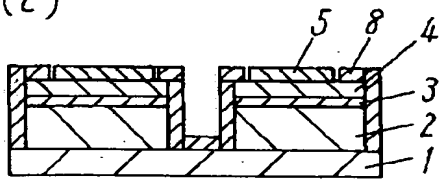

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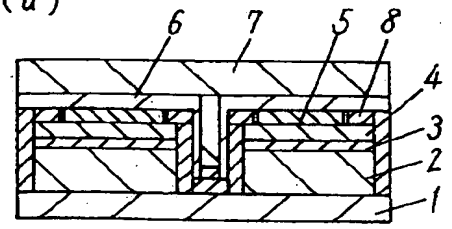
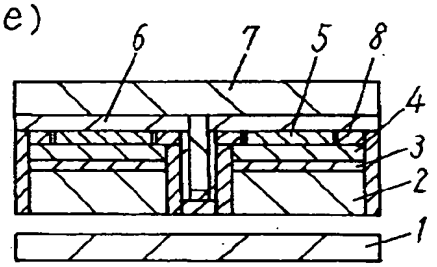
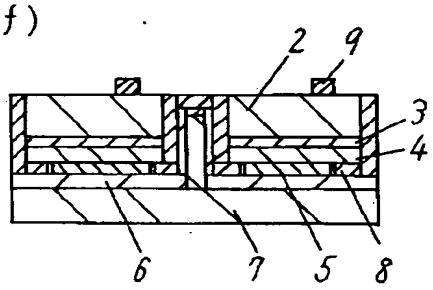


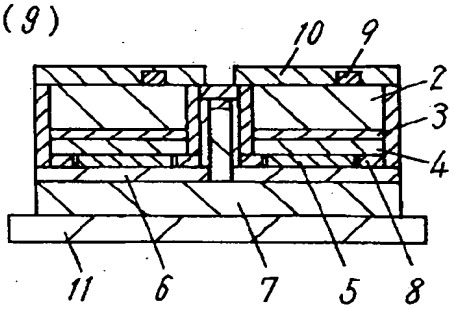
(e)



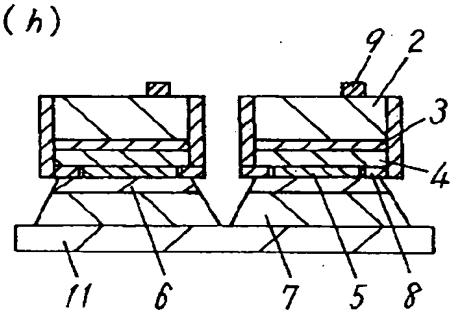
(f)



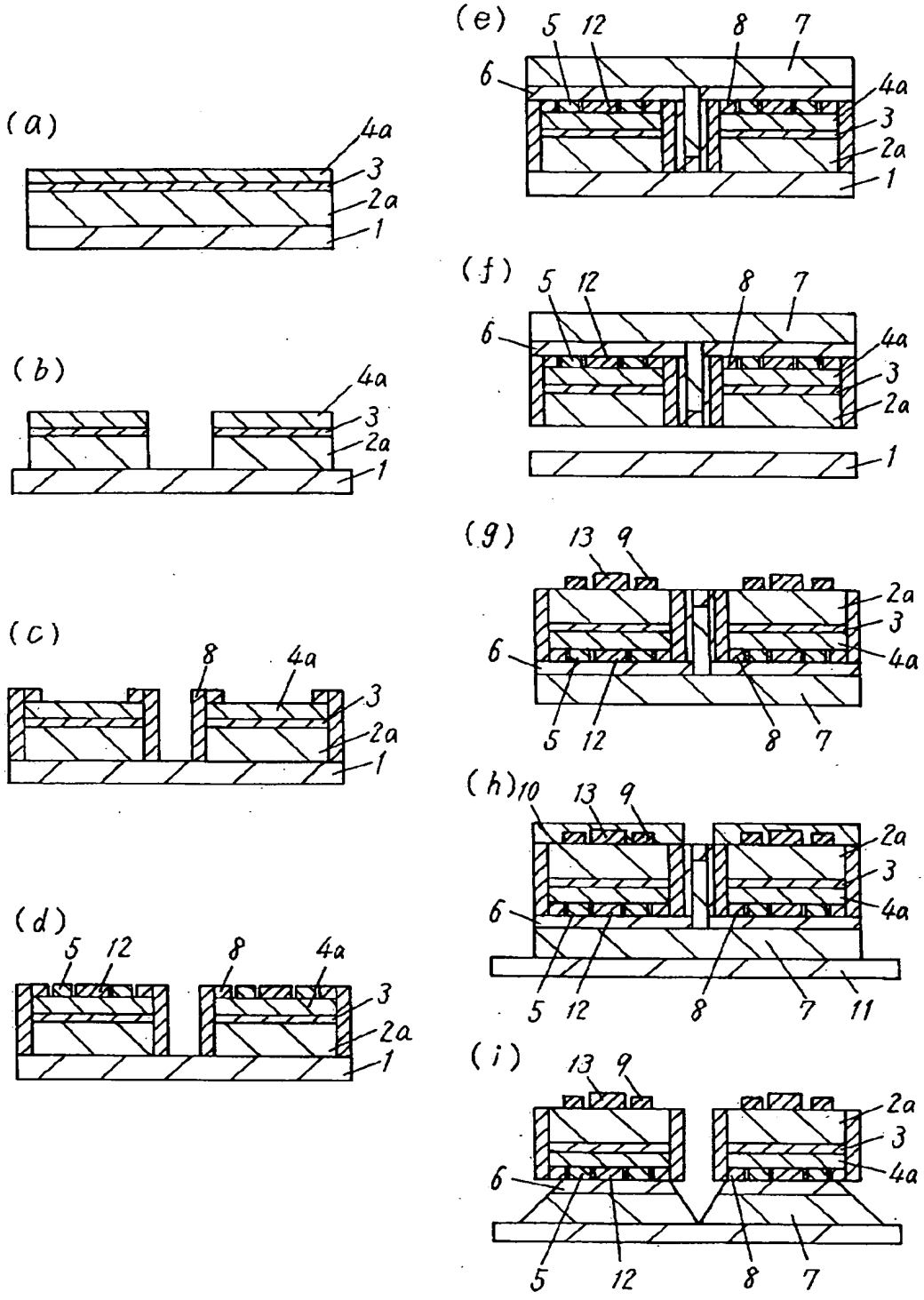
(g)



(h)



【図3】〔FIG. 3〕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(b)
4a
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2a
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(c)
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4a
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2a
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(d)
5
12
8
4a
3
2a
1
(e)
5
12
8
7
6
4a
3
2a
1
(f)
5
12
8
7
6
4a
3
2a
1
(g)
13
9
2a
3
6
4a
5
12
8
7
(h)
10
13
9
2a
3
6
4a
5
12
8
7
11
(i)
13
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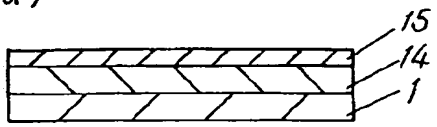
3
6
4a
5
12
8
7

【図4】 [FIG. 4]

(a)



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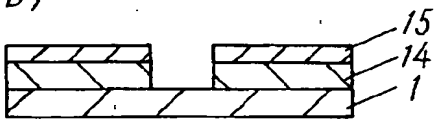
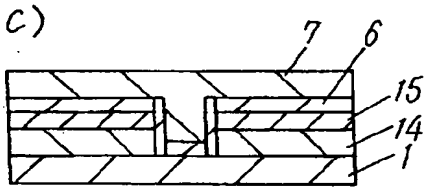
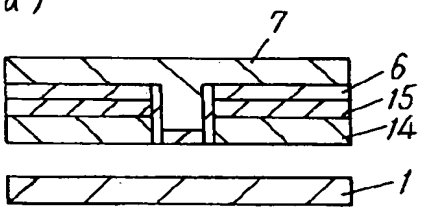


(c)



(d)



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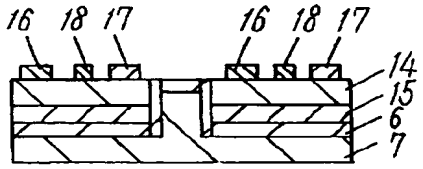
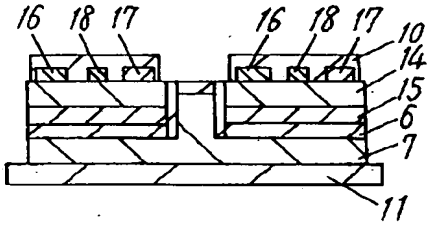
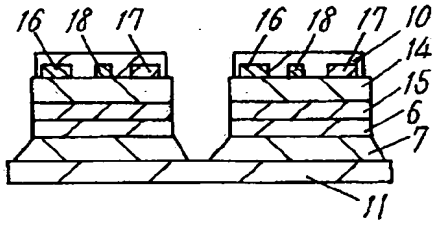


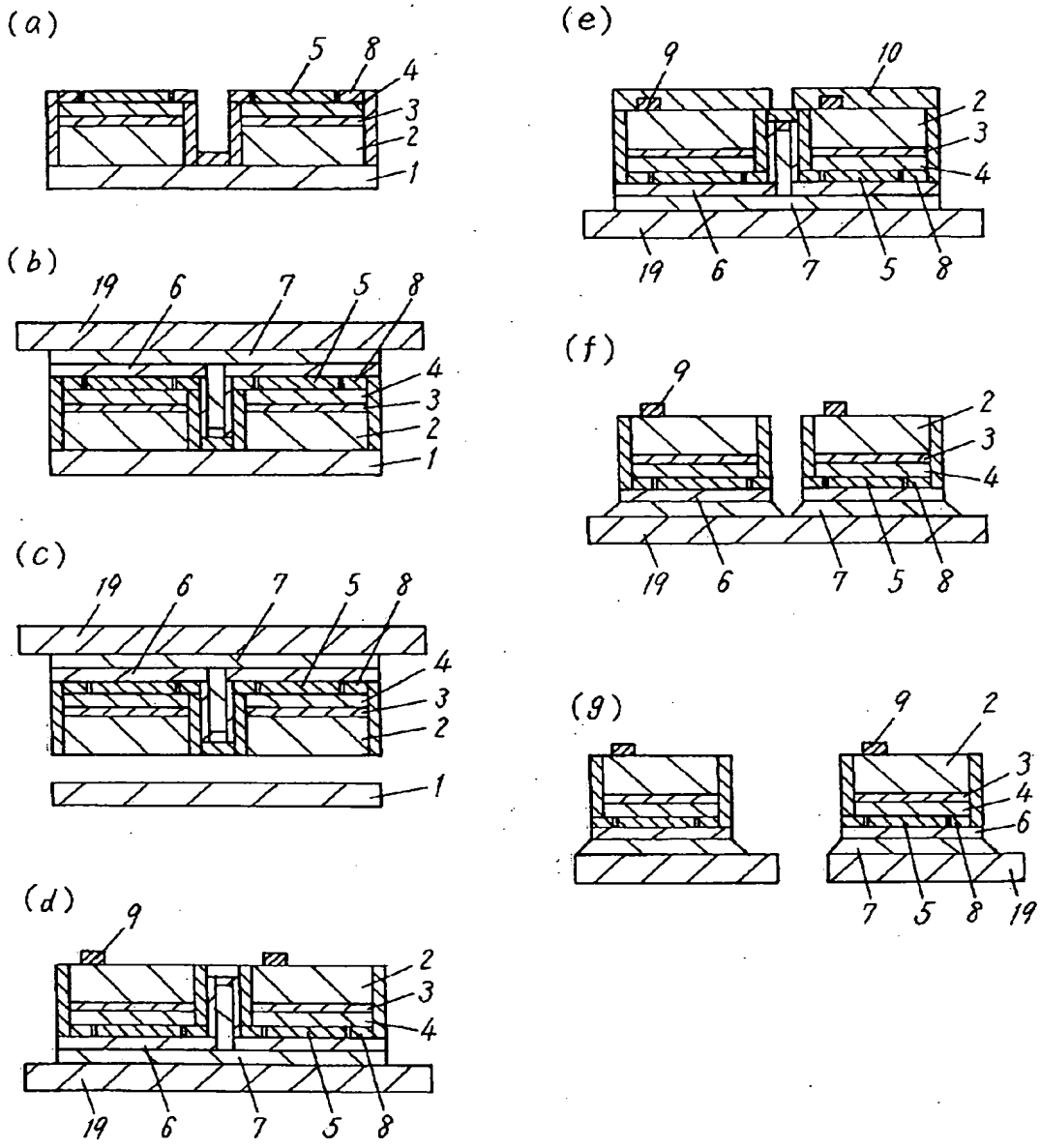
(f)



(g)

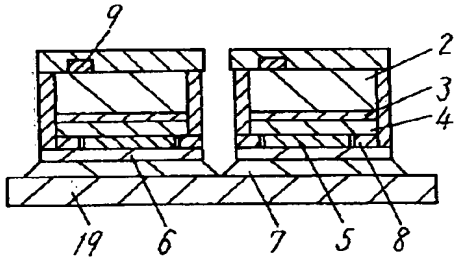


【図5】〔FIG. 5〕


(a)
5 8 4 3 2 1
(b)
19 6 7 5 8 4 3 2 1
(c)
19 6 7 5 8 4 3 2 1
(d)
9 2 3 4 19 6 7 5 8
(e)
9 10 2 3 4 19 6 7 5 8
(f)
9 2 3 4 19 6 7 5 8
(g)
9 2 3 4 6 7 5 8 19

【図6】 [FIG. 6]

(a)



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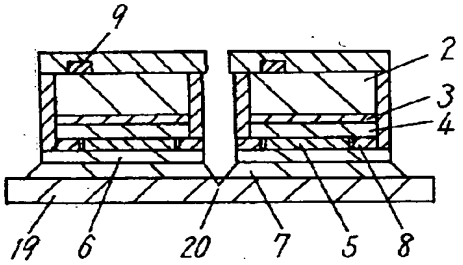
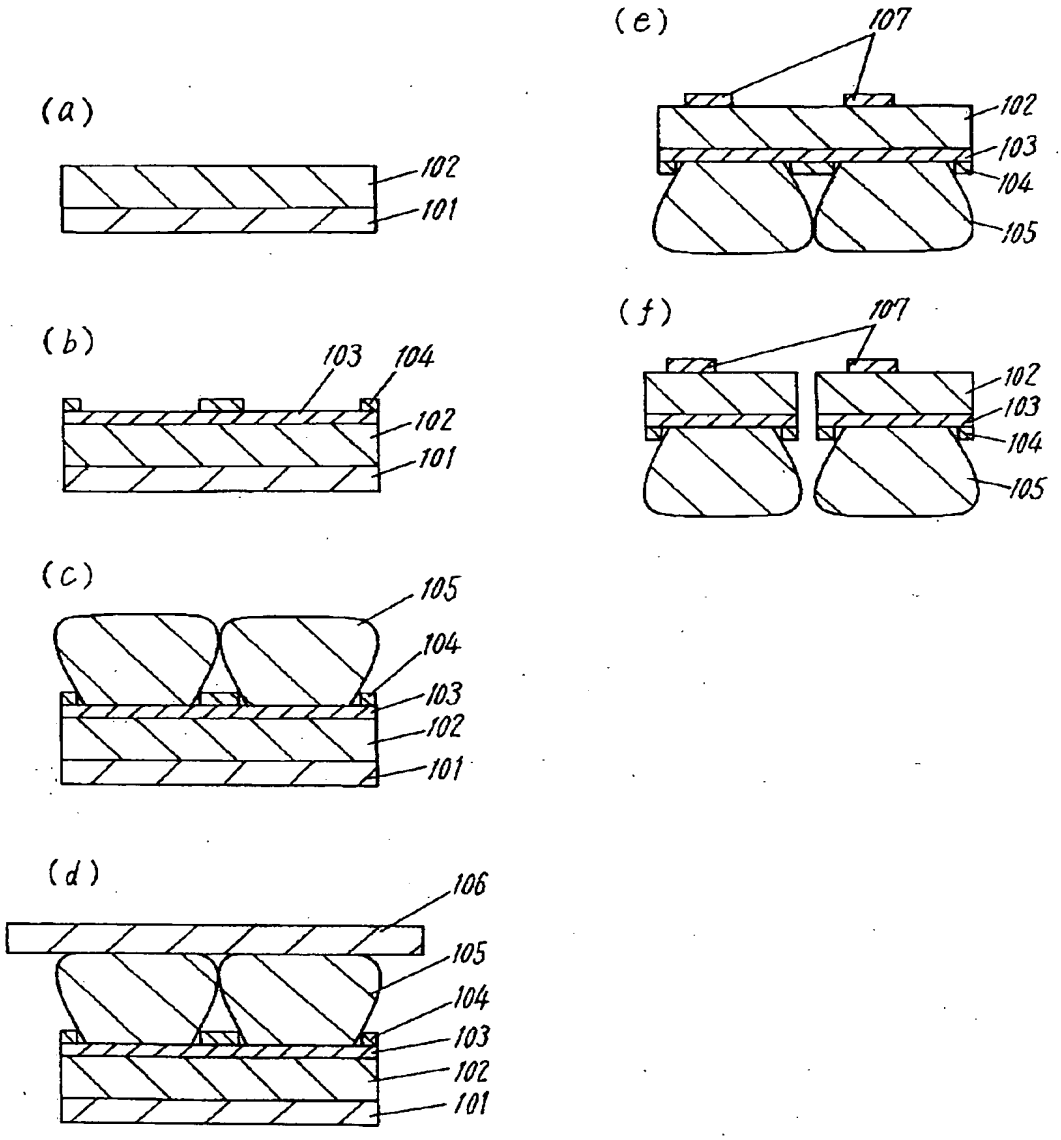


【図7】〔FIG.7〕


(a)
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(b)
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(c)
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(d)
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105
104
103
102
101
(e)
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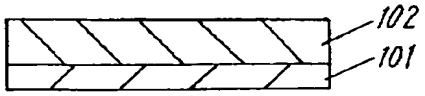
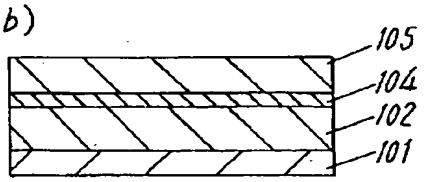
104
105
(f)
107
102
103
104
105

【図8】 [FIG. 8]

(a)



(b)



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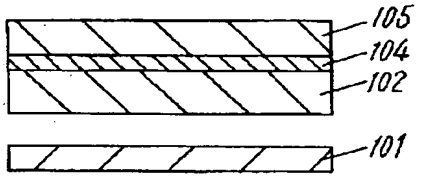

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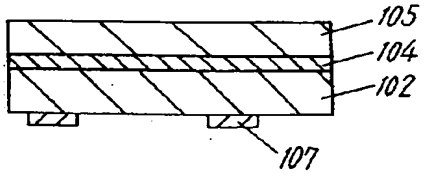

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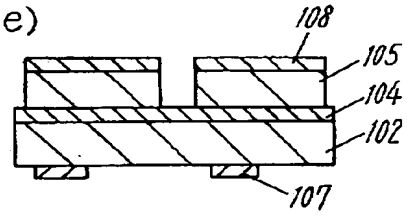

(f)